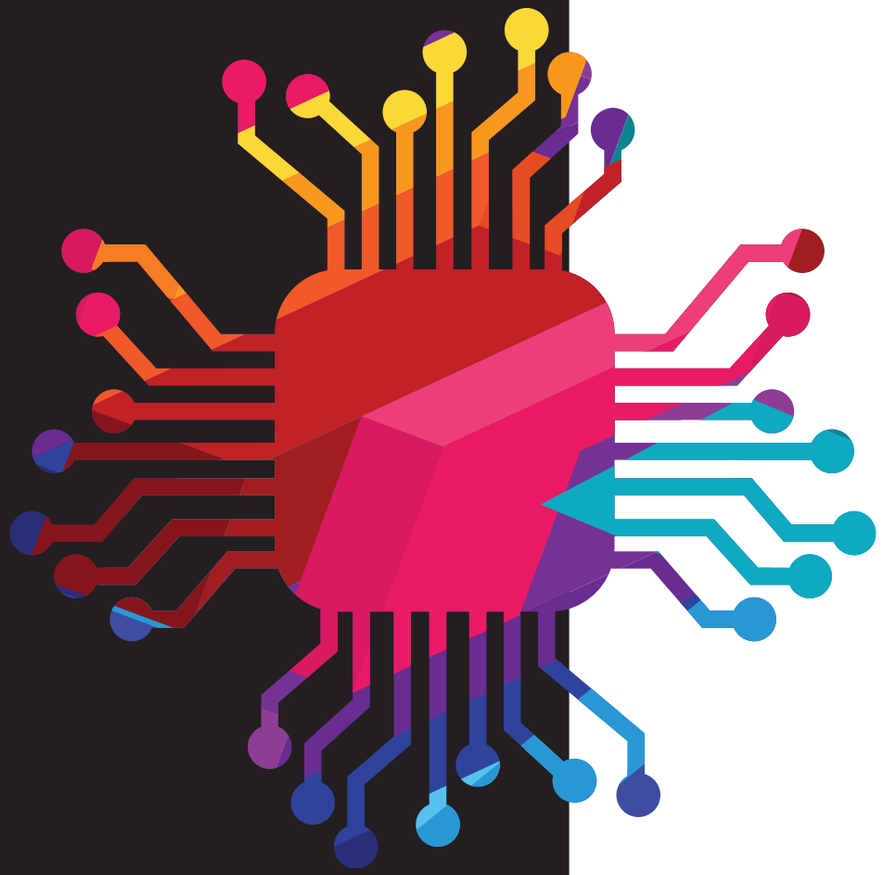
Schedule

MAY
26-27
2019



dgcon 2019 Spring Edition

Experts Sharing Knowledge

By

dgtronix Design Innovators

dgcon
Experts Sharing Knowledge

dgtronix Design Innovators

DNIX
ASIC Prototyping Platforms

27th Maskit St. Herzliya-Pituach, Corex House, 3rd floor
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MAY 26, 2019

Spring Edition

08:00-09:00 Registration and Breakfast
Sign in, make yourself a cup of coffee, and meet your fellow engineers

09:00-09:30 Opening speech
Dudi Tash, CEO, *Dgtronix*

09:30-10:00 Essential Design Tips using High Speed Connectors
Dudi Tash, CEO, *Dgtronix*

10:00-11:30 Measurement-Based, Harmonic Balance VRM Model
Steve Sandler, Managing Director, *Picotest - Keynote Speaker*

11:30-11:45 Break

11:45-12:30 Simulation to Measurement Challenges on PAM4 for 400GB
Hee-Soo Lee, Product owner, *Keysight Technologies*

12:30-13:30 Lunch

13:30 - 15:00 Typical Cavity Resonators in PCBs and their Impact on Signal and Power Integrity
Dror Haviv, Signal/Power Integrity and Electromagnetism Specialist, *Rafael*

15:00 - 15:15 Break

15:15 - 16:00 SerDes Channel Design and Characterization
Danilo Di Febo, SIMULIA Solution Consultant Specialist, *Dassault Systems*

16:00 - 16:45 The Return Loss (RL) Evolution - Effective Return Loss (ERL) to substitute RL
Liav Ben-Artsi, Staff Signal Integrity Manager, *Marvell*

MAY 27, 2019

Spring Edition

08:00-09:00 Registration and Breakfast
Sign in, make yourself a cup of coffee, and meet your fellow engineers

09:00-09:30 Opening speech
Dudi Tash, CEO, *Dgtronix.*

09:30-11:00 Power Related Noise in Distributed Systems
Steve Sandler, Managing Director, *Picotest*

11:00-11:15 Break

11:15-12:00 A Practical Guide to Signal Integrity: From Simulation to Measurement
Mike Resso, Signal Integrity Application Scientist, *Keysight Technologies*

12:00-12:45 Distributed Decoupling Capacitors Application for PDN Designs of Fine Pitch BGA Products
Alex Manukovsky, Technical lead of the Signal & Power Integrity, *Intel*
Shimon Mordooch, R&D Project Manager, *Harmonic Video Networks*

12:45-13:45 Lunch

13:45-15:15 Deep dive into the SerDes compliance requirements, modeling and analysis methods of the most popular protocol
Cristian Filip, Product Architect High-Speed Analysis Products, *Mentor Graphics*

15:15-15:30 Break

15:30-17:00 Understanding the PCI Express 4.0/5.0 Test Methodologies and Measurement Challenges
Dan Froelich,Director of Systems Engineering and Domain Expert, PCIe, *Tektronix*

17:00-17:15 Lottery & Summary