
dgcon 2015
Agenda
Dan Accadia, Herzliya
dgcon 2015

DAY 1

9.11.15

Time	Description
8:00-9:00	Registration & Gathering
9:00-9:30	Opening Lecture - Nonhomogeneous current distribution in Power Vias Mr. Dudi Tash, SI/PI Expert, Dgtronix
9:30-10:30	Session 1: A crash course in power integrity principles Dr. Eric Bogatin, Dean, Signal Integrity Academy, Teledyne LeCroy
10:30-10:45	Break
10:45-11:45	Session 2:The real problem in PDN Design, the Bandini Mountain Dr. Eric Bogatin, Dean, Signal Integrity Academy, Teledyne LeCroy
11:45-13:00	Session 3: The most important design solutions for a robust PDN Dr. Eric Bogatin, Dean, Signal Integrity Academy, Teledyne LeCroy
13:00-14:00	Lunch
14:00-14:45	A New Calibration Method for Characterization of PCB Insertion Loss Mr. Mike Resso, Signal Integrity Application Scientist in the Component Test Division of Keysight Technologies
14:45-15:30	High-speed systems: What makes or breaks a 25Gbps channel Dr. Davi Correia, Signal Integrity Engineer, Molex
15:30-15:45	Break
15:45-16:45	The Impact Of Conductors' Power Dissipation On The PCB's Temperature Rise Mr. Dror Haviv, Signal/Power Integrity and Electromagnetism Specialist, Rafael
16:45-17:15	Common-Mode Noise Suppression Using Metamaterials Mr. Shai Sayfan-Altman, Application Engineer, ANSYS
17:15-17:30	Closing Speech

DAY 2

10.11.15

Time	Description
8:00-9:00	Registration & Gathering
9:00-9:15	Opening Lecture Mr. Dudi Tash, SI/PI Expert, Dgtronix
9:15-10:00	On Radiation Emissions from high-speed PCBs Dr. Avri Frenkel, Representative and Tech Support of CST in Israel, Anafa Elctro Magnetic Solutions Ltd
10:00-11:00	Incorporating COM into an SI analysis methodology Mr. Cristian Filip, Product Marketing Manager High Speed Analysis Products SDD, Mentor Graphics Corporation
11:00-11:15	Break
11:15-13:00	PCB Material and Copper Foil Considerations for Signal Integrity Mr. Jeff Loyer, Signal and Power Integrity Product Manager, Altium
13:00-14:00	Lunch
14:00-14:45	PCB Material and Copper Foil Considerations for Signal Integrity Mr. Jeff Loyer, Signal and Power Integrity Product Manager, Altium
14:45-15:30	Robust De-embedding techniques – practical solutions to lab correlation challenges Mr. Alex Manukovsky, Technical lead, Signal & Power Integrity team, Intel
15:30-15:45	Break
15:45-16:15	EMC & SI In Electro Optic Defense And Commercial Systems Mr. Eli Recht, Chief Engineer, EMC Department, ELOP/Elbit
16:15-16:45	Testing 25Gbps for 802.3bj Mr. Liav Ben Artsi, Signal Integrity Group Manager, Marvell
16:45-17:15	100G and 400G Optical Ethernet and general Datacom testing requirements Mr. John Calvin, Ultra Performance Instrument Planner/DataCom Segment Manager, Tektronix
17:15-17:30	Closing Speech

DAY 3 DGCON+ 11.11.15

Time	Description
8:30-9:30	Registration & Gathering
9:30-13:00	Boot Camp with Eric Bogatin Dr. Eric Bogatin, Dean, Signal Integrity Academy, Teledyne LeCroy

S-parameter boot camp

Session 1:
- what are S-parameters
- where do they come from
- viewing Touchstone files in the frequency and time domains with a free tool
- the most important features of return and insertion loss

Session 2:
- Ripples in return and insertion loss
- Dips in insertion loss
- Differential S-parameters
- Converting from SE to diff S-parameters

Session 3:
- SDD21 and attenuation
- SDD21 and eye diagrams
- Building channel models form S-parameter elements
- SDD11 and TDR of a channel

High speed serial link boot camp

Session 1:
- The four problems with channels
- Engineering losses
- Differential pairs and tight or loose coupling
- Cross talk and differential pairs

Session 2:
- Engineering discontinuities
- Designing transparent vias
- How long a stub is too long
- Channel models and eye diagram

Session 3:
- What is jitter and the time interval error
- Jitter from ISI and the PDN
- Random jitter
- Equalization and opening eyes

13:00-14:00	Lunch
14:00-15:00	Q&A
15:00-15:15	Closing Speech